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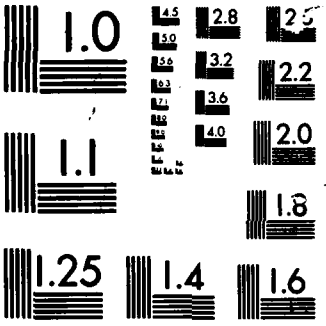


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# Synchronizer Failure in A/D Converters*

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## ABSTRACT

Analog-to-digital converters that must produce a valid output in a specified period of time are subject to synchronizer failure. Three types of A/D converters are examined: flash converters, clocked successive approximation converters, and self-timed successive approximation converters. Lower bounds on their worst-case conversion time as a function of the fault probability are derived.

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*This research was supported by the Defense Advanced Research Projects Agency under contract number N00014-80-C-0622.

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# Synchronizer Failure in A/D Converters

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**Abstract:** Analog-to-digital converters that must produce a valid output in a specified period of time are subject to synchronizer failure. Three types of A/D converters are examined: flash converters, clocked successive approximation converters, and self-timed successive approximation converters. Lower bounds on their worst-case conversion time as a function of the fault probability are derived.

## 1. Introduction

The finite gain-bandwidth product of the comparators used in analog-to-digital (A/D) converters gives rise to fundamental limits on the speed of various converter architectures. While the average delay of an A/D converter can be made quite fast, the worst-case conversion time of any A/D converter is unbounded [1]. This is because there is always some probability that, if the output of an A/D converter is used in a synchronous digital computer system, a fatal synchronizer fault can occur. Our objective is to express a lower bound on the "worst-case" A/D conversion time as a function of this fault probability.

The synchronizer problem in digital systems has been studied for many years [2-14]. Briefly stated, the problem occurs when an asynchronous signal is gated into a clocked system. The clocked system must decide, in a specified period of time, the state of the asynchronous input. The circuit that must make this decision is called a synchronizer.

The synchronizer problem occurs because the synchronizer circuit can take an arbitrarily long time to decide, in marginal cases, whether the input is above or below a given reference standard. In most physical circuits this phenomenon can be attributed to the gain-bandwidth tradeoff. Since, at any given time, the input can be arbitrarily close to the comparator reference, the amplification needed to turn this difference into a full logic swing can be arbitrarily large. For a circuit with a fixed gain-bandwidth product, the delay incurred in achieving this enormous amplification can grow arbitrarily large. If the circuit is required to produce a valid output by a certain time, then there is a finite probability $P$ that the output will be invalid (not a logic one or a logic zero) at that time. $P$ decreases exponentially with the time that synchronizer is given to make its decision. Many ingenious techniques, such as adding hysteresis or noise, have been tried to circumvent the synchronizer problem, but the dilemma appears fundamental. The standard solution has become to just wait a sufficient period of time that $P$ is acceptably small.

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If one could build an A/D converter that could be guaranteed to always produce a valid digital output in a bounded amount of time, then one could use this converter to build a fault-free synchronizer. Indeed, the typical synchronizer is nothing more than a one bit A/D converter. This is reason to suspect that the perfect A/D converter does not exist. Tognoni has examined this problem experimentally and observed metastable problems in a commercial A/D converter [15]. In the remainder of this paper we will examine synchronizer problems in A/D converters theoretically, deriving lower bounds on the latency of the A/D conversion as a function of the required reliability.

## 2. The Model

There are many circuit modules in a typical A/D converter but all A/D converters make use of one or more comparators. We focus our attention, in this paper, on the speed of the comparator.

There are basically two types of comparators. The simplest takes the form of a high gain amplifier; the output voltage of which limits at zero and the positive power supply voltage. We normalize the power supply voltage to 1. If the gain of the high gain amplifier is $A$, then the output of the comparator is undefined (not a logic 0 or 1) if $|v_{\rm in} - v_{\rm ref}| < 1/(2A)$. $v_{\rm in}$ is the input voltage and $v_{\rm ref}$ is the comparator reference voltage. Thus, there is a finite input voltage range over which the output takes an infinitely long time to settle and if we compute the average comparator response time over all input voltages (all voltages are assumed equally likely) then the average response time diverges to infinity. The delay of a well-designed multistage amplifier takes the form $T_{\rm delay} = \tau \ln A$, where $\tau$ is a constant of the technology. (A simple way to view this is to cascade two high-gain amplifiers. The gains multiply and the delays add.)

A bistable (or regenerative) comparator circuit has better average delay properties. Figure 1 illustrates a simple bistable CMOS comparator circuit clocked on $\phi$. The delay $T_{\rm delay}$ of this circuit is roughly

$$T_{\rm delay} = -\tau \ln |v_{\rm in} - v_{\rm ref}|, \tag{1}$$

where $v_{\rm in}$ and $v_{\rm ref}$ are normalized to the power supply voltage and $\tau$ is roughly equal to the inverse of the gain-bandwidth product for the individual inverters (transistors $M_1$ through $M_4$). We normalize the delay to $\tau$. Rewriting (1) in normalized form, we have

$$T_{\rm delay} = -\ln |\Delta|, \tag{2}$$

where we have defined

$$\Delta \equiv v_{\rm in} - v_{\rm ref}. \tag{3}$$

The delay of this amplifier diverges only logarithmically with $\Delta$ and therefore has a finite average delay. We will confine our study to this second type of comparator.

The average speed of the comparator is a function of the distance between adjacent bits. For an $N$ bit converter, the (normalized) voltage difference $v_{\rm bit}$ between adjacent bits is

$$v_{\rm bit} = 2^{-N}. \tag{4}$$

The binary fractions range from 0 to $1 - 2^{-N}$.

It is convenient to partition the input voltage into a digital part plus an analog residue. We re-express $v_{in}$ as $v_{in} = V + v$ where $-v_{bit} < 2v \leq v_{bit}$ and $V$ is the ideal voltage representation of an exact $N$-bit binary fraction, such as the four-bit numbers $0.1011_2$ or $0.0001_2$. The conversion time is always a function of $v$ and may, or may not, be a function of $V$, depending on the converter architecture.

In the remainder of this paper we will investigate two types of delay. The average delay $T_{avg}$ is defined as the average of the conversion delays which would be observed if one averaged the times required to perform a large number of conversions, where we have assumed that all input voltages $v_{in}$ are equally likely. We define the worst-case delay $T_{worst-case}$ in terms of the fault probability $P$. If we require $P = 0$ then $T_{worst-case} \rightarrow \infty$. What we mean by the worst-case conversion time is that if we observe a very large number of conversions $M$ of randomly selected input voltages (uniform distribution) and we throw out the slowest $PM$ of these conversions as causing faults, then the worst-case conversion time $T_{worst-case}$ is the slowest conversion time in the remaining set of $(1 - P)M$ better conversions.

## 3. Flash Converter

For the flash converter, there exists some comparator for which the input voltage is within $\pm v_{bit}/2$ of the reference voltage. For this comparator we may write $\Delta = v$. Assume that all values of $v$ are equally likely over the interval $(-v_{bit}/2, v_{bit}/2]$. The average value of $T_{delay}$ is given by

$$T_{avg} = -\frac{1}{v_{bit}} \int_{-v_{bit}/2}^{v_{bit}/2} \ln|v| dv. \tag{5}$$

Solving, we obtain

$$T_{avg} = 1 + (N + 1) \ln 2 \tag{6}$$

for the flash converter. The minimum average delay increases linearly with $N$ for a given technology.

If $v = 0$, $T_{delay} \rightarrow \infty$. Given a specified value of $T_{delay}$, there is some range of $v$ over which the comparator output fails to settle in time. When this happens we say that we have a fault. Let us denote the interval of fault causing voltages by $-\delta < 2v \leq \delta$. The probability of a fault $P$ is given by

$$P = \delta / v_{bit}. \tag{7}$$

We can bound the worst-case delay $T_{worst-case}$ to be

$$T_{worst-case} > \ln \frac{1}{v_{bit} P}. \tag{8}$$

The interpretation of (8) is that if we perform conversions of $M$ independent input voltages, we expect $T_{delay}$ to be greater than $T_{worst-case}$ for at least $PM$ conversions. Solving (8), we obtain

$$T_{worst-case} > N \ln 2 - \ln P. \tag{9}$$

The value of $P$ for which $T_{\text{worst case}} = T_{\text{avg}}$ is $1/2e$. Note that the dependence of the delay on $N$ becomes relatively less important as $P$ is made smaller.* Figure 2 illustrates (9) for three different values of $P$.

## 4. Clocked Successive Approximation Converter

For a clocked successive approximation A/D converter, the average latency is simply $N$ times the clock period. The length of the clock period depends on the fault probability one is willing to accept. The probability of fault in a noiseless successive approximation converter is simply the probability of not successfully completing a conversion on any one clock cycle. Note that this probability is, because the system was assumed ideal and noiseless, just the probability of faulting on the $N$th conversion. This was derived for the flash converter. Since there are $N$ conversions, we have

$$T_{\text{worst-case}} > N^2 \ln 2 - N \ln P. \tag{10}$$

Equation (10) is plotted in Fig. 3.

## 5. Self-timed Successive Approximation Converter

We can observe from (1) that the comparator delay is a function of the initial voltage difference. As pointed out by H.-S. Lee [16], not all conversion steps in a successive approximation converter can be within $\pm v_{\text{bit}}/2$ of the reference voltage. This means that some conversions will be fast and some slow. Figure 4 illustrates the block diagram of a self-timed successive approximation converter. The asynchronous logic for this figure was designed by Mr. Tam-Anh Chu and is documented in [17]. The comparator is balanced at the beginning of each conversion. The end of each conversion is sensed by a mutual exclusion circuit [18]. (Because our analysis ignores the significant overhead time of balancing the amplifier, sensing the completion, and changing $v_{\text{ref}}$, these bounds are not as tight as the ones in the previous section. Thus comparisons of self-timed and clocked successive approximation converters should be done with care.)

On each conversion $k$, a binary number $B_k$ is tested. Let $D_k \equiv B_k - V$ be the difference between the present test value $B_k$ and the final binary voltage. $D_k$ can be either positive or negative and is bounded by $|D_k| \leq 2^{-k}$, where $1 \leq k \leq N$. The delay $T_k$ of the $k$th conversion (considering only the comparator delay contribution) is given by

$$T_k = -\ln |D_k - v|. \tag{11}$$

Summing over all $N$ conversions,

$$T_{\text{delay}} = -\sum_{k=1}^{N} \ln |D_k - v|. \tag{12}$$

* While the average performance of the amplifier type comparator is poor, the worst-case performance is similar to that of the bistable comparator. This is because, for the same level of reliability, they both are required to provide amplification on the order of $1/(P v_{\text{bit}})$.

The average conversion time $T_{\rm avg}$ is found by averaging (12) over all $v$ and all $V$. The averaging over $v$ can be done in closed form. Given a particular $V$,

$$T_{\rm avg}(N,V) = \sum_{k=1}^{N} T_{Dk}, \tag{13}$$

where we have defined the conversion time for one bit $T_{Dk}$ as

$$T_{Dk} \equiv -\frac{1}{v_{\rm bit}} \int_{-v_{\rm bit}/2}^{v_{\rm bit}/2} \ln|D_k - v| dv. \tag{14}$$

Solving(14), we obtain

$$T_{Dk} = \begin{cases} 1 - \left\{ \left( \left| \frac{D_k}{v_{\rm bit}} \right| + \frac{1}{2} \right) \ln\left( |D_k| + \frac{v_{\rm bit}}{2} \right) - \left( \left| \frac{D_k}{v_{\rm bit}} \right| - \frac{1}{2} \right) \ln\left( |D_k| - \frac{v_{\rm bit}}{2} \right) \right\} & \text{for } D_k \neq 1 \\ 1 - \ln\left( \frac{v_{\rm bit}}{2} \right) & \text{for } D_k = 0 \end{cases} \tag{15}$$

$D_k$ is a function of $V$ and $N$. Averaging (13) over all $V$ we obtain

$$T_{\rm avg}(N) = 2^{-N} \sum_{V=0}^{1-2^{-N}} \sum_{k=1}^{N} T_{Dk}. \tag{16}$$

The worst-case delay is given by

$$T_{\rm worst-case}(N) > \max_{0 \le V \le 1} \sum_{k=1}^{N} -\ln|D_k - v_{\rm bit} P|. \tag{17}$$

A program was written to preform exhaustive analysis, for all $V$ from $N = 1$ to 14, on (16) and (17). For (17), $P$ was set to 0.1, $10^{-5}$, and $10^{-9}$. Figure 5 illustrates the worst-case and average behavior of the self-timed successive approximation converter. Table 1 gives the numbers $V$ which caused the worst-case performance in (17). In many cases there are several numbers which cause equivalently slow behavior. The smallest of these is listed. Empirically, numbers of the form ...010101 always caused worst-case behavior. For $N$ in the region 14–20 and $P$ in the region of $10^{-9}$ to $10^{-12}$, the lower bound on the self-timed successive approximation converter speed was about five times slower than a flash converter constructed in the same technology.

Table 1. Worst-case $V$ versus $N$

| $N$ | $V$ (base 2) |
|---|---|
| 2 | 0.01 |
| 3 | 0.011 |
| 4 | 0.0101 |
| 5 | 0.01101 |
| 6 | 0.010101 |
| 7 | 0.0110101 |
| 8 | 0.01010101 |
| 9 | 0.011010101 |
| 10 | 0.0101010101 |
| 11 | 0.01101010101 |
| 12 | 0.010101010101 |
| 13 | 0.0110101010101 |
| 14 | 0.01010101010101 |

## 6. Conclusions

Three types of converters were studied with respect to average and worst-case delay. In all cases, the worst-case latency was shown to increase with increasing reliability. Note that while latency is a function of $P$, the throughput need not decrease with decreasing $P$, providing one is willing to add extra pipeline hardware to give the synchronizers time to settle.

We can divide A/D applications into two classes. Those in which latency is important (such as industrial control applications in which the A/D is in a feedback path with, say, a microprocessor) and those in which throughput is important (such as for image processing). For the first class of applications, one can anticipate that catastrophe avoidance will mandate high reliability requirements. This implies a small $P$, in conflict with system stability requirements for low latency. For pipelined signal processing applications, additional pipeline stages can easily be added to reduce $P$ to an acceptable level.

One of the more intriguing results of this study is that the self-timed successive-approximation converter begins to become competitive, in terms of speed, with flash converters for very low $P$ and large $N$. This is because, for low $P$, both the flash and self-timed successive-approximation converters spend most of their time working on the one hard ($v \ll v_{bit}$) bit that must be assumed to be there.

## 7. Acknowledgements

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## Figures





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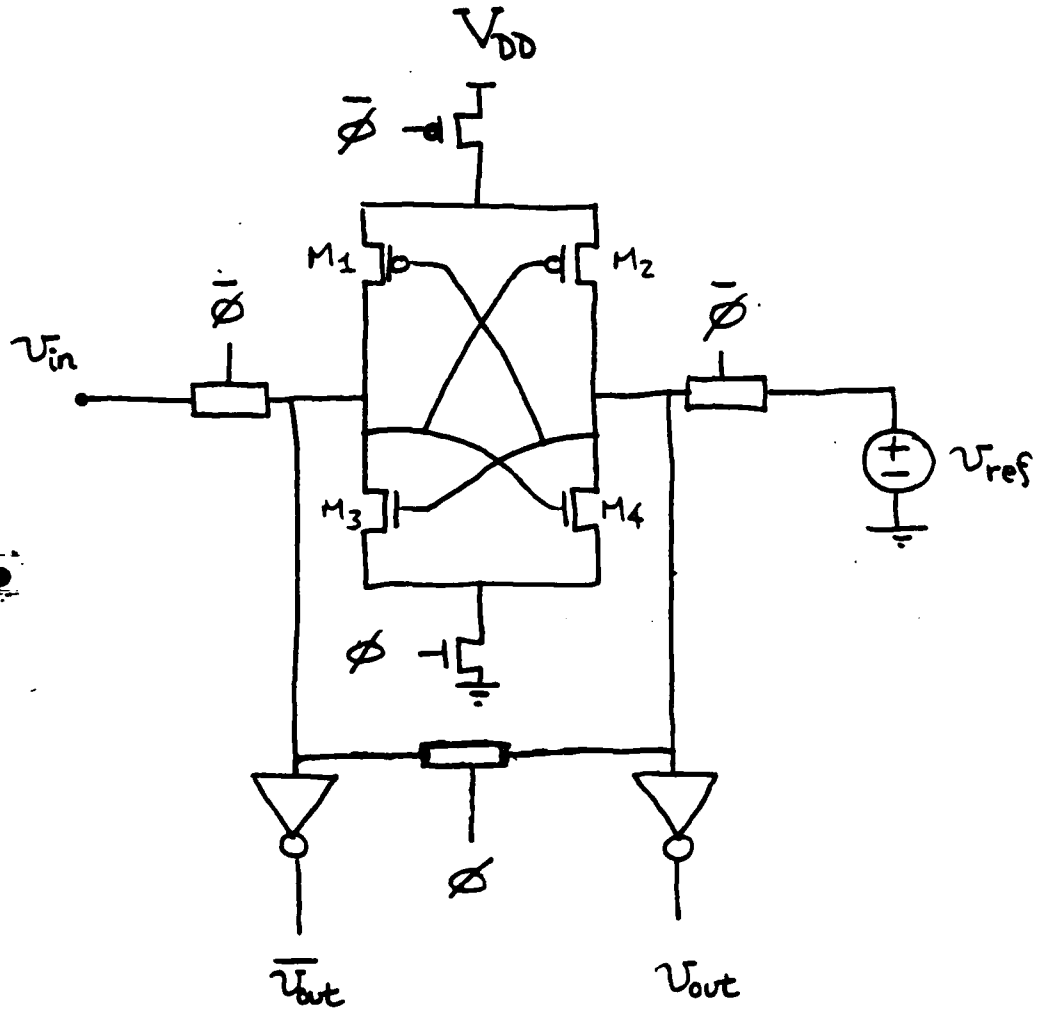
$V_{DD}$
$\bar{\phi}$
$M_1$
$M_2$
$\bar{\phi}$
$\bar{\phi}$
$v_{in}$
$v_{ref}$
$M_3$
$M_4$
$\phi$
$\phi$
$\bar{v}_{out}$
$v_{out}$

Fig 1

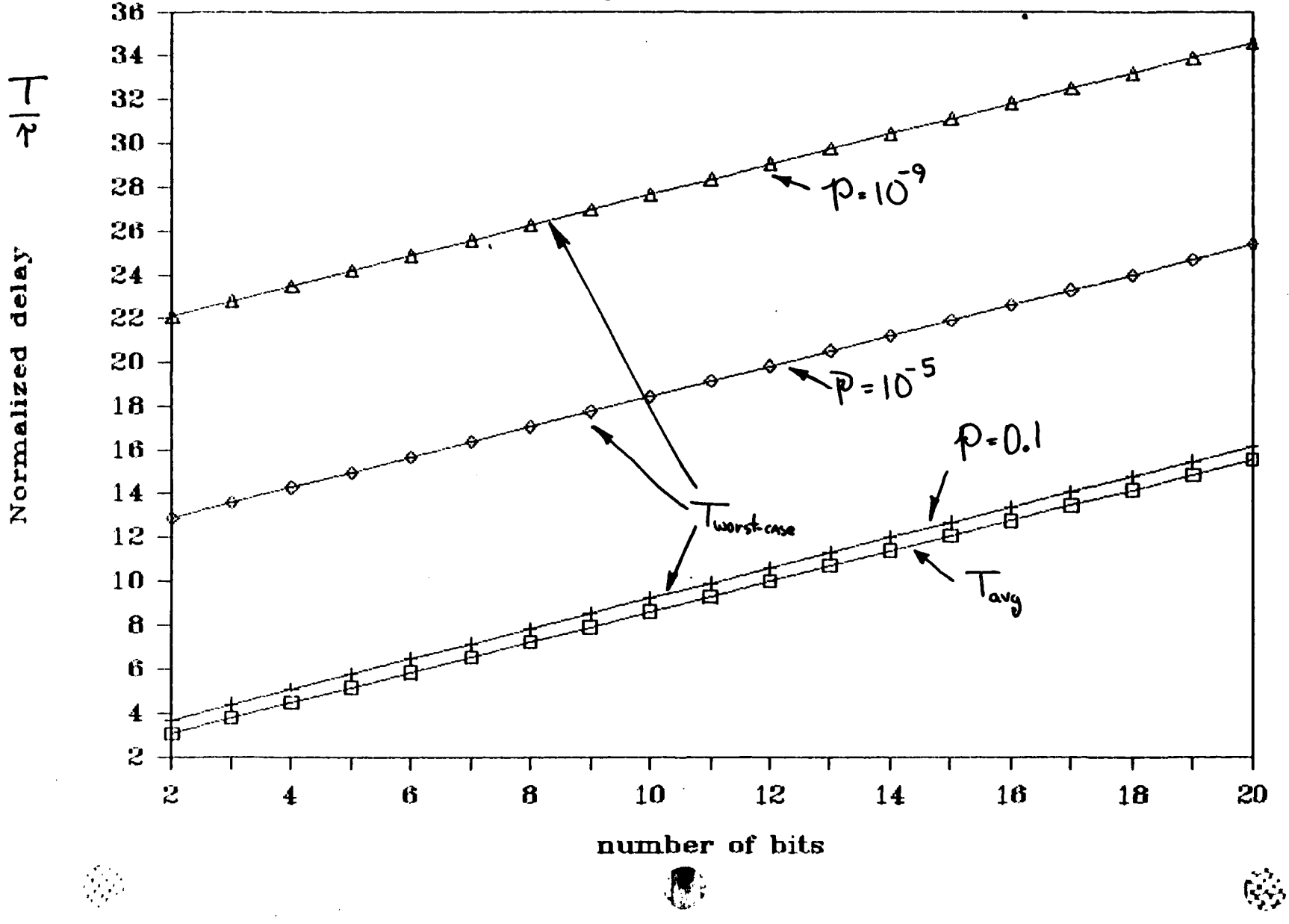
Flash Converter
Avg, p(f)=.1, 1e-5, 1e-9
Normalized delay
T/τ
36
34
32
30
28
26
24
22
20
18
16
14
12
10
8
6
4
2
2
4
6
8
10
12
14
16
18
20
number of bits
p=10^-9
p=10^-5
p=0.1
T worst-case
T avg

FIG 2

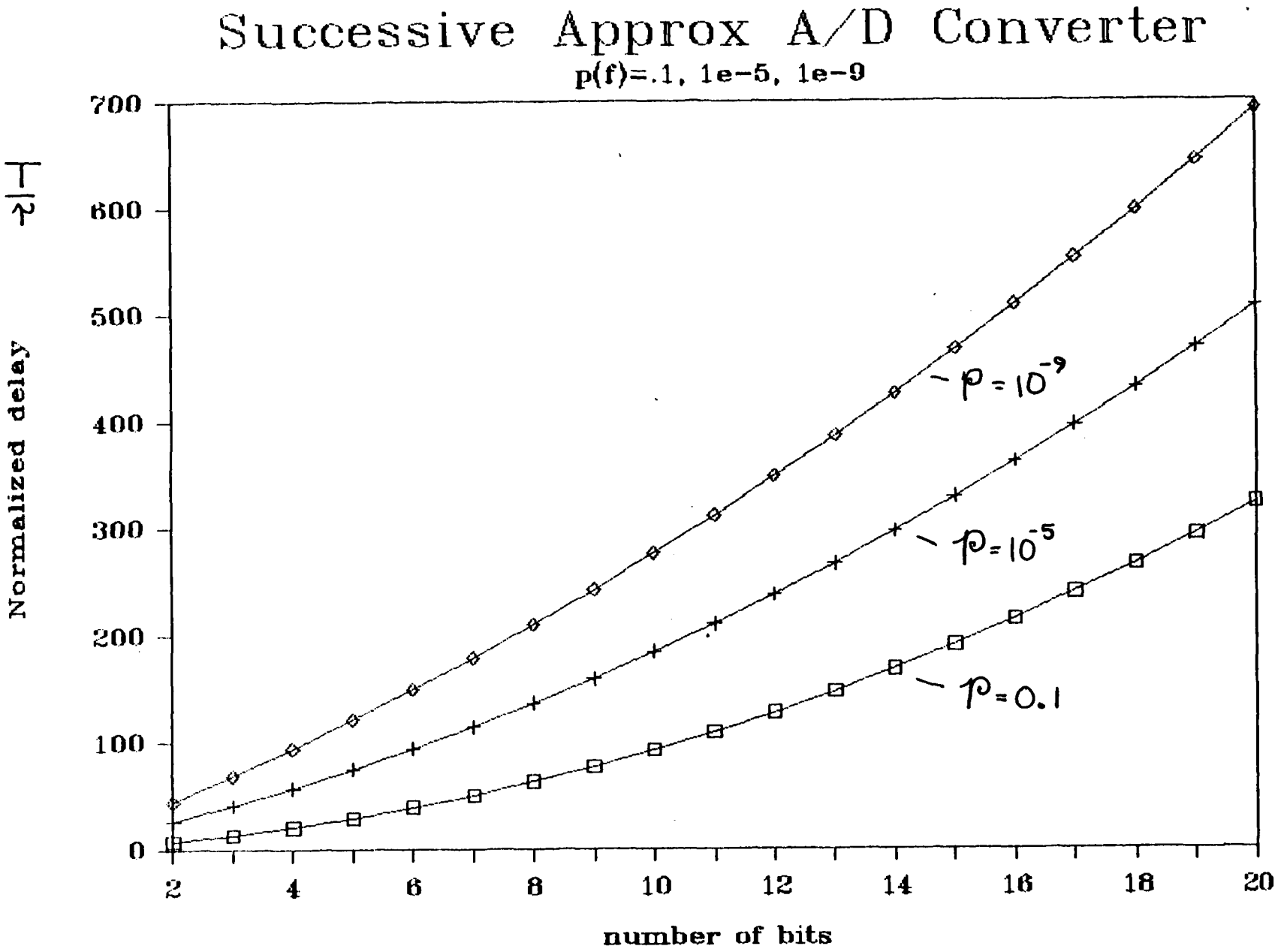
Successive Approx A/D Converter
p(f)=.1, 1e-5, 1e-9
Normalized delay
700
600
500
400
300
200
100
0
2
4
6
8
10
12
14
16
18
20
number of bits
p = 10^-9
p = 10^-5
p = 0.1

FIG 3

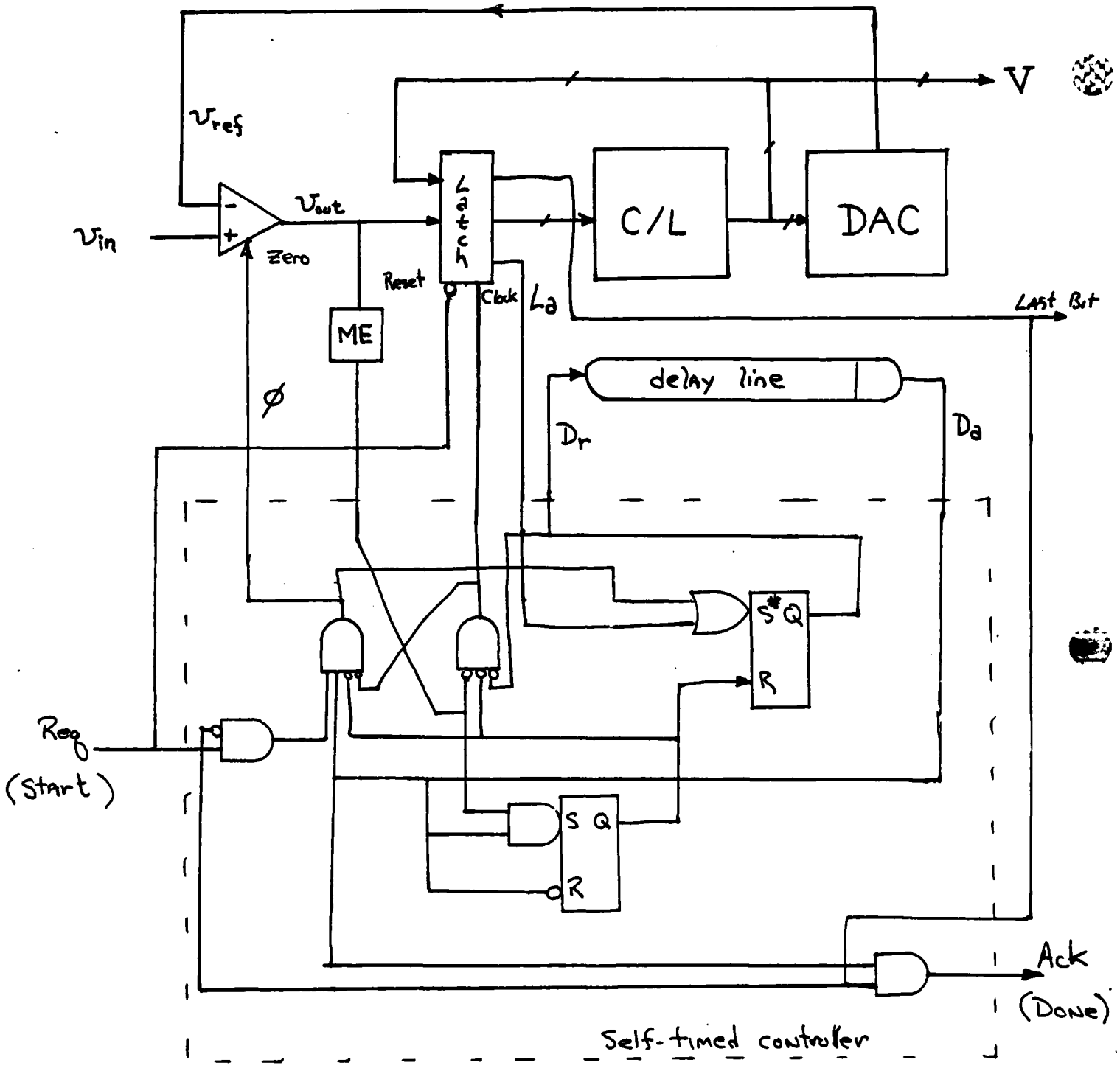
V
$V_{ref}$
$V_{out}$
$V_{in}$
Zero
Latch
C/L
DAC
Reset
Clock
$L_a$
Last Bit
ME
$\phi$
delay line
$D_r$
$D_a$
S Q
R
S Q
R
Req
(Start)
Ack
(Done)
Self-timed controller

FIG 4

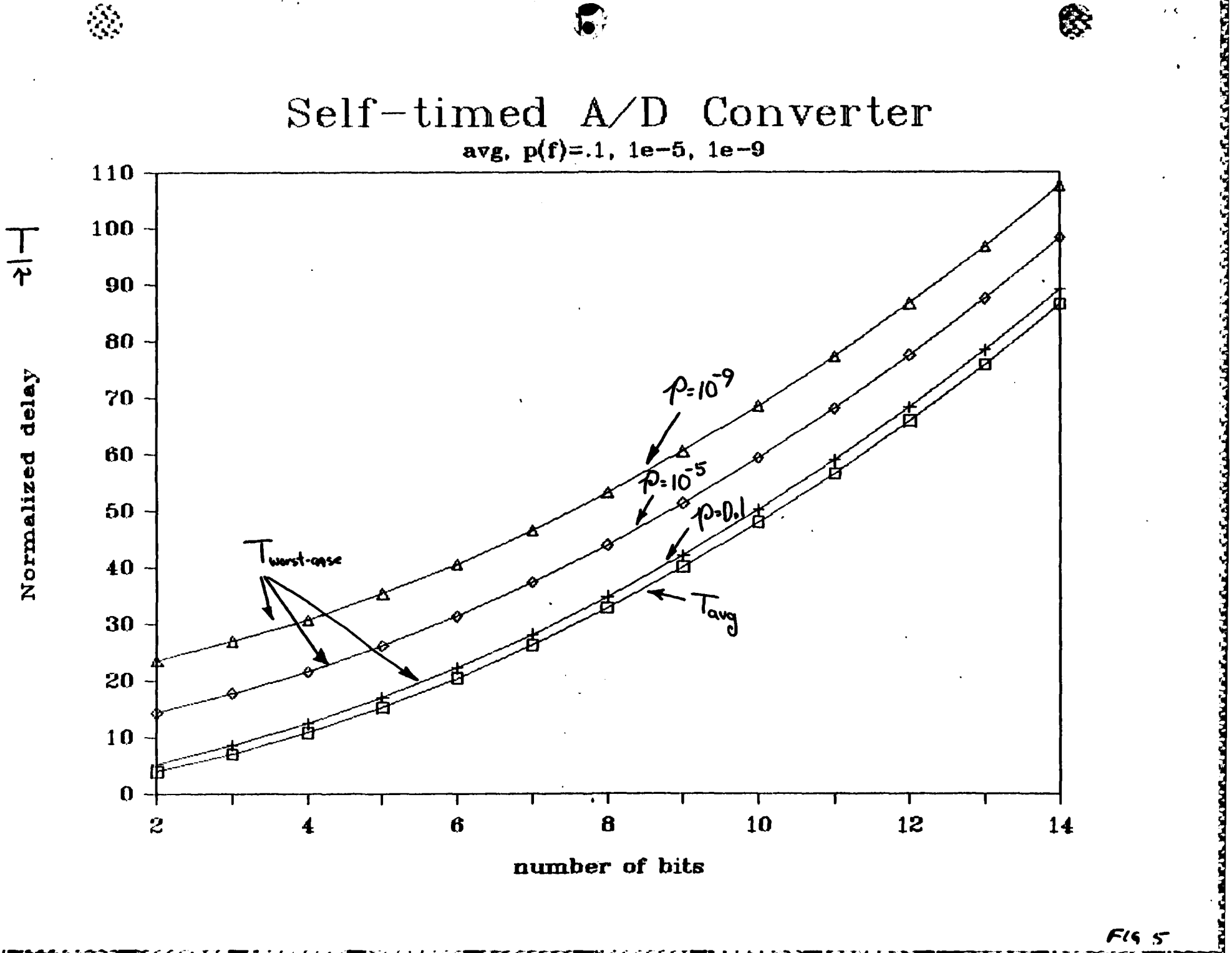
Self-timed A/D Converter
avg. p(f)=.1, 1e-5, 1e-9
Normalized delay
number of bits
110
100
90
80
70
60
50
40
30
20
10
0
2
4
6
8
10
12
14
$p=10^{-9}$
$p=10^{-5}$
$p=0.1$
$T_{worst-case}$
$T_{avg}$

FIG 5

END

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